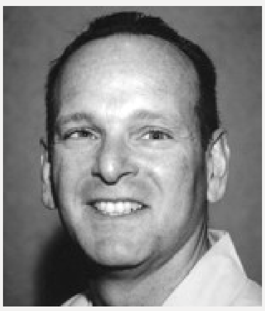
CROSSOVER SPACE:
EMERGING CONCEPTS FOR SPACE SYSTEMS

The days of "traditional" space missions (large satellites and risk avoidance on electronics) has been replaced by "small space", risk management, and a rapidly growing commercial presence.

This topical day discusses two sides of the burgeoning changes:

- Selective emerging electronic technologies that provide potential enabling characteristics for the new regime of space, and,
- Alternative concepts for systems risk management and evaluation.



Ken LaBel
NASA-NEPP
Topical Day Chair

TOPICAL DAY PROGRAM
MONDAY 17TH OF SEPTEMBER

08:20-08:30
INTRODUCTION

08:30-09:35

NON-VOLATILE MEMORIES FOR SPACE: THE THREAT OF IONIZING RADIATION
Marta Bagatin, University of Padova

An overview of radiation effects in non-volatile memories will be provided, with emphasis on Flash and Phase Change memories. Total ionizing dose and single event effects in NAND and NOR Flash technologies will be presented, discussing possible issues in both the memory cells and the control circuitry, and the underlying mechanisms. Technology scaling trends in Flash memories will be analyzed over the last decade, going from floating gate planar cells to recent 3D architecture. The synergies between SEE and TID, as well as the impact of radiation on long term performances, such as retention and endurance, will also be covered. Recent observations of upsets in PCM cells due to very highly ionizing particles impinging at an angle will be discussed. Finally, a brief overview of the state of other emerging technologies, such as ReRAM and ST-MRAM, will be provided.

09:35-10:05 **MORNING BREAK**

10:05-11:10

WIDE-BANDGAP SEMICONDUCTORS IN SPACE: APPRECIATING THE BENEFITS BUT UNDERSTANDING THE RISKS
Jean-Marie Lauenstein, NASA/GSFC

Dr. Jean-Marie Lauenstein, NASA Goddard Space Flight Center, will present the radiation challenges of adopting wide-bandgap semiconductors for space applications. Wide-bandgap devices are attractive for space applications due to improved performance such as faster switching speeds, lower power losses, and their ability to operate at higher temperature as compared with their silicon counterparts. Their tolerance to total ionizing dose levels (> 100 krad(Si)) further enhances the desirability of these technologies. This short course will focus on silicon carbide and gallium nitride power rectifying, switching, and RF devices as these technologies are now readily available commercially. The radiation hardness assurance issues presented by the heavy-ion radiation environment will be discussed. Effects include both catastrophic failure and cumulative degradation, challenging the practice of risk avoidance through derating and possibly requiring new test method standards unless or until truly radiation-hardened devices become available. The course will conclude with a brief survey of additional wide-bandgap technologies such as diamond and gallium oxide.

11:10-12:15

NEW SPACE AND AUTOMOTIVE INDUSTRIAL RADIATION PARADIGMS

Philippe Roche, ST Microelectronics

Dr. Philippe Roche, STMicroelectronics Technical Fellow and High-Reliability R&D Director, will discuss radiation challenges with fast adoption of sub-28nm technologies for large commercial space and safety critical automotive programs. The radiation paradigm for risk management has already changed with shorter development programs (<5 years to effective use in harsh environments) and stronger requirements for ultra-performance in space and for smart autonomous driving (<20% of perf. loss vs. commercial parts). That trend might modify the links between semiconductor companies, aerospace industries, agencies and laboratories (paces, methods, roadmaps). Radiation experts have also now to handle new failure modes in leading-edge technologies (FDSOI, FinFET, PCM, ToF imagers), stronger impacts of single event transients (in clock trees, varactors), stronger coupling effects across reliability fail modes and test methods (TID, BTI, TID post-OLT) and broader circuit functions to harden while not compromising performances (analog, RF, sensors, GHz processors). Additional complexities arise from ultra-low error counting during ground testing (with robust SOI) vs. non-negligible error rate potentially in very-large systems in field (B's of latches), as well as with larger amounts of radiation-tolerant circuits to produce (10's to 100K's parts) vs. growing variabilities to control (natively or with embedded monitors for self-adjustments).

12:15-13:45 **LUNCH at "Imagine"**

13:45-15:00

FROM COTS TO SPACE GRADE ELECTRONICS: WHICH IS THE BEST FOR YOUR MISSION?

Robert Baumann, TI

After a brief overview of chronic radiation exposure effects (total ionizing dose and neutron/proton dose) and single-event effects (SEEs) that plague microelectronics in space, we consider unintentional radiation performance enhancements that have occurred as a natural consequence of technology scaling. "Natural" technology hardening is one of the reasons consumer-off-the-shelf (COTS) parts can, in some cases, be used in commercial space applications. We then provide a couple of real-world examples of commercial manufacturing variations and demonstrate how these impact microelectronic radiation sensitivity. We conclude with a discussion of the value of lot control, screening, and custom packaging methods and how their use improves product reliability while ensuring that radiation performance meets mission needs.

15:00-15:30 **AFTERNOON BREAK**

15:30-16:45

NEXT GENERATION PROCESSING FOR SPACE SYSTEMS

Raphael Some, NASA/JPL

Future NASA missions will require autonomous capabilities and onboard science data processing in order to overcome communications limitations including link bandwidth and round trip speed of light delays. Future United States Air Force (USAF) missions have similar requirements. The joint NASA-USAF High Performance Space Computing project (HPSC) is developing a radiation hardened, fault tolerant, modular processing element, termed "The Chiplet" to address these future needs. The chiplet concept seeks to develop a family of processors and associated system software that enables "plug and play" (PnP) "system in a package" (SIP) implementations of advanced rad hard computing architectures at an affordable development and deployment cost. The HPSC Chiplet project is the first element of this processor family and, if successful, is expected to lead to the development of an "ecosystem" comprising additional heterogeneous processor chiplets, memories, network elements, operating systems, middleware libraries, software development systems, and the packaging technologies required to achieve 2.5 and 3D SIP space based computing and avionics systems. In this talk we will discuss the concepts behind the HPSC Chiplet, the Chiplet architecture and specifications, the envisioned HPSC ecosystem, current status and future plans.